3035C
Wideband RF Digitizer
PXI Module

Operating Manual

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About this manual

This manual applies to instruments with software driver issues of 3.0 and higher.

This manual explains how to set up and configure an Aeroflex 3035C wideband RF digitizer PXI module. Where necessary, it refers you to the appropriate installation documents that are supplied with the module.

This manual provides information about how to configure the module as a stand-alone device. However, one of the advantages of Aeroflex 3000 Series PXI modules is their ability to form versatile test instruments, when used with other such modules and running 3000 Series application software.

Getting Started with afDigitizer (supplied on the CD-ROM that accompanies each module (see Associated documentation)) explains how to set up and configure a 3030 Series RF digitizer with a 3010 Series RF synthesizer module to form a high performance digitizer instrument. Using the digitizer soft front panel and/or dll or COM object supplied, the modules form an instrument that provides the functionality and performance of an integrated, highly-specified RF digitizer, but with the adaptability to satisfy a diverse range of test or measurement requirements.

Intended audience

Users who need to configure and operate the 3035C wideband RF digitizer to down-convert and digitize RF signals.

This manual is intended for first-time users, to provide familiarity with basic operation. Programming is not covered in this document but is documented fully in the help files that accompany the drivers and associated software on the CD-ROM.

Driver version

This PXI RF module is designed to be used with the latest software driver version supplied on the Aeroflex 3000 Series PXI Modules CD-ROM part no. 46886/028. Operation with earlier versions of driver software is not supported.

Structure

Associated documentation

If you want to…	Refer to…
Find information about soft front panels, drivers, application software, data sheets, getting started and operating manuals for this and other modules in the 3000 Series.	**PXI Modules CD-ROM** Part no. 46886/028 Supplied with the module
Install modules into a rack, interconnect them, power up and install drivers.	**3000 Series PXI Modules Common Installation Guide** Part no. 46882/663 On paper, on the CD-ROM and on www.aeroflex.com
Set up a populated chassis ready for use.	**3000 Series PXI Modules Installation Guide for Chassis** Part no. 46882/667 On paper, on the CD-ROM and on www.aeroflex.com
Set up and use the universal PXI application for system configuration and operation.	**PXI Studio User Guide** Part no: 46892/809 On the CD-ROM and on www.aeroflex.com
Set up and use a signal generator application for 3010 Series and 3030 Series modules.	**Getting Started with afDigitizer** Part no. 46892/676 On the CD-ROM and on www.aeroflex.com

Preface

The PXI concept

VXI and GPIB systems meet the specific needs of instrumentation users but are often too large and expensive for mainstream applications. PC-based instrumentation may cost less but cannot meet the environmental and operational requirements of many systems.

PXI (PCI Extensions for Instrumentation) is based on CompactPCI, itself based on the PCI standard. PCI was designed for desktop machines but CompactPCI was designed for industrial applications, and features a rugged Eurocard format with easy insertion and removal. PXI adds to the CompactPCI specification by defining system-level specifications for timing, synchronization, cooling, environmental testing, and software. While PXI extends CompactPCI, it also maintains complete interoperability so that you can use any CompactPCI-compliant product in a PXI system and vice versa. PXI also makes use of Windows software, VXI timing and triggering, and VXIplug&play instrument drivers to provide powerful and affordable systems.

Abbreviations/acronyms

ACLR	Adjacent Channel Leakage Ratio
ACP	Adjacent Channel Power
ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-Digital Converter
AM	Amplitude Modulation
ARB	Arbitrary Waveform Generator
CW	Continuous Wave
DAC	Digital-to-Analog Converter
dB	Decibels
dBc	Decibels relative to the carrier level
dBm	Decibels relative to 1 mW
FFT	Fast Fourier Transform
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
GND	Ground
IQ	In-phase/Quadrature
LO	Local Oscillator
LSTB	List Strobe
LVDS	Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
Pk-Pk	Peak-to-Peak

PXI	PCI eXtensions for Instrumentation
F	Radio Frequency
RMS	Root Mean Square
SFP	Soft Front Panel
SMA	SubMiniature version A (connector)
SMB	SubMiniature version B (connector)
TDMA	Time Division Multiple Access
TRIG	Trigger
TTL	Transistor-Transistor Logic
UUT	Unit Under Test
VCO	Voltage-Controlled Oscillator
VHDCI	Very High Density Connector Interface
VSWR	Voltage Standing-Wave Ratio
VXI	VMEbus Extension for Instrumentation

Chapter 1 GENERAL INFORMATION

Introduction

Welcome to the operating manual for the 3035C Wideband RF Digitizer PXI module.

The 3035C, when used with a 3010 Series PXI RF synthesizer module, forms a compact wideband RF digitizer that occupies four slots in a 3U PXI chassis.

Applications

The 3035C down-converts and digitizes RF signals. It converts an analog RF waveform presented at its RF port into a series of amplitude- and phase-corrected digital IF or IQ data pairs at the rear-panel PCI and front-panel data interfaces. Software supplied with the module allows for spectrum analysis of the digitized signals.

The 3035C can be used in RF test and measurement systems used in development or manufacturing. Applications span all areas of radio communications.

PXI Express compatibility

The 3035C is a hybrid slot-compatible PXI-1 peripheral module.

Wide frequency coverage

The module provides continuous frequency coverage from 250 kHz to 6 GHz. A linear single-stage down-converter converts input signals to an IF centered on 187.25 MHz.

Input range and accuracy

Input level control is provided by electronic switched attenuation, which helps to maximize the usable dynamic range. Good level accuracy and repeatability make the module ideal for high-volume manufacturing.

Wide bandwidth

The 3035C produces a 90 MHz wide digitized IF signal, with amplitude and phase correction applied across 33 MHz. Full-rate digital IF or decimated IQ data can be output via LVDS, useful for real-time emulation. Data can also be captured to internal memory and read over the PCI bus.

For narrowband signal analysis, the module provides internal digital down-conversion and decimation. Lowering the sample rate allows longer events to be captured. The module contains digital resampling filters that allow you to set the sample rate, as well as numerous preset values associated with common digital communications standards.

Signal routing

A configurable routing matrix provides flexibility in how you interconnect signals on the PXI backplane and the LVDS front-panel input. Predefined routing scenarios can be selected, or your own matrix settings stored and recalled.

Triggering and synchronization

The module synchronizes to an external 10 MHz signal (generally supplied by a 3010 Series RF synthesizer). Triggering is external, from the PXI backplane or directly from the front-panel LVDS connector or SMB TTL input, or internal, from the internal timer or level trigger.

List mode

In list mode, up to 128 internal hardware settings can be pre-calculated and stored, providing fast switching of frequency whilst maintaining RF output accuracy. List addresses are sourced externally or from an internal counter, possibly driven by the test application controlling the module. In production, list mode enables faster testing and simplified programming.

Software

The module is supplied with a VXI PNP driver and soft front panel for use as a self-contained module. An instrument-level soft front panel is also provided, together with a dll and COM object, combining the controls of the 3035C together with the 3010 Series RF synthesizer. Refer to *Getting Started with afDigitizer* (part no. 46892/676) supplied on the PXI Modules CD-ROM part no. 46886/028. An FFT spectrum analyzer measurement suite is supplied, and optional signal analysis components are available to measure power, modulation quality and spectra to recognized communications standards.

PXI Studio, also supplied with the module, configures your PXI modules as logical instruments using an intuitive and powerful graphical interface. Currently, PXI Studio provides comprehensive signal generator, digitizer and spectrum analyzer applications and optional analysis plugins to suit various communications standards.

RF Investigator, also supplied with the module, is an application that provides combined operation of all Aeroflex 3000 Series modules from a single user interface, especially useful for acceptance testing.

Deliverable items

- 3035C Wideband RF Digitizer PXI module
- PXI Modules CD-ROM (part no. 46886/028), containing soft front panels, drivers, application software, data sheets, getting started and operating manuals for this and other modules in the 3000 Series
- *3000 Series PXI Modules Common Installation Guide*, part no. 46882/663
- *3000 Series PXI Modules Installation Guide for Chassis*, part no. 46882/667
- SMA connector cable, part no. 43139/590 (2 off)

Cleaning

Before commencing any cleaning, switch off the chassis and disconnect it from the supply. You can wipe the front panel of the module using a soft cloth moistened in water, taking care not to wet the connectors. Do not use aerosol or liquid solvent cleaners.

Putting into storage

If you put the module into storage, ensure that the following conditions are not exceeded:

Temperature range:	–20 to +70°C (–4 to +158°F)
Humidity:	5 to 93%, non-condensing

Chapter 2 INSTALLATION

WARNING

Initial visual inspection

Refer to the 3000 Series Common Installation Guide 46882/663.

CAUTION

Handling precautions

Refer to the 3000 Series Common Installation Guide 46882/663.

Hardware installation

Installing the module into the PXI chassis

Refer to the 3000 Series Common Installation Guide 46882/663 and Installation Guide for Chassis 46882/667.

Connector care and maintenance

How to connect and torque an SMA connector

1. First, ensure that the mating halves of the connector are correctly aligned.
2. Next, engage the threads of the nut and tighten it by hand, ensuring that the mating halves do not move relative to each other.
3. Then use a torque wrench to tighten the connector, in order to ensure consistent matching and to avoid mechanical stress.

   Torque settings for connectors are:

   0.56 Nm test torque (development use, semi-permanent installations)

   1 Nm final torque (permanent installations)

Never use pliers to tighten connectors.

CAUTION

Overtightening will cause damage!

SMA

Clean connectors regularly, using a cotton bud dipped in isopropyl alcohol. Wipe within the connector cavity, then use a dry cotton bud to finish off. Check for any deposits.

Do not use other cleaners, as they can cause damage to the plastic insulators within the connectors.

Cap unused connectors.

PCI

Protect PCI connector pins by keeping modules in their original packing when not fitted in the rack.

Chapter 3 OPERATION

Front-panel connectors

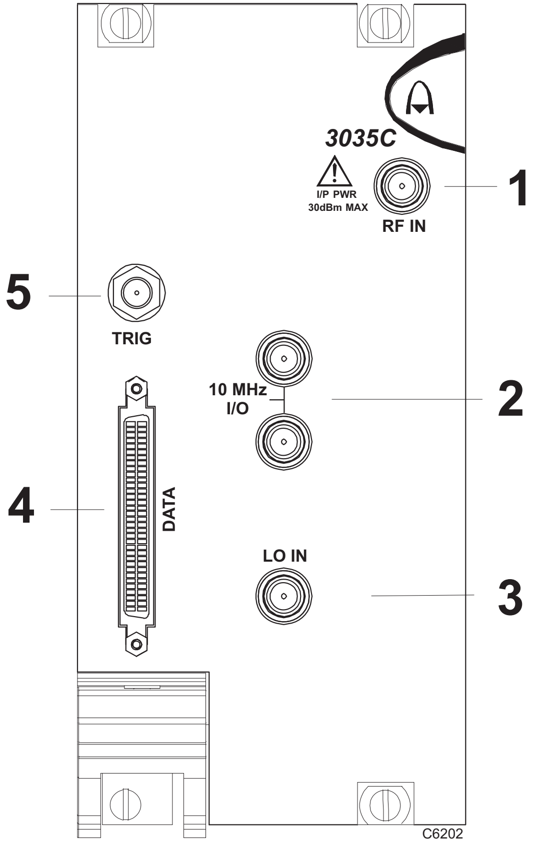


Fig. 3-1 3035C front panel

1	RF IN	+30 dBm max. (0 dB input attenuation). SMA socket, 50 Ω.
2	10 MHz I/O	Two SMA I/O sockets in parallel. **Input** Ext frequency standard input for sampling clock. 1.0 to 4 V pk-pk into 50 Ω. **Output** Link-through from input.
3	LO IN	1.5 to 3 GHz, nominally 0 dBm. SMA socket, 50 Ω.
4	DATA	68-way VHDCI connector for LVDS data I/O, 14-bit IQ digital data output. See Appendix A for details.
5	TRIG	TTL +ve or –ve edge. SMB socket, 50 Ω.

CAUTION

Maximum safe power
RF input: **+30 dBm** continuous (0 dB input attenuation)

Soft front panel (af3030_sfp)

The soft front panel provides a graphical interface for operating the module. It is intended for testing and diagnosing, for demonstration and training, and for basic operation of the module. It represents most of the functions available in the instrument driver. It is not, however, a comprehensive application suitable for measurements; for this, use the afDigitizer dll, the afcomDigitizer COM object, or PXI Studio.

Installation

The soft front panel is installed during the driver installation process (refer to the *3000 Series PXI Modules Common Installation Guide*, part no. 46882/663).

Access the soft front panel from the Windows Start menu under *Programs\Aeroflex\PXI Module Front Panels\AF3030 Soft Front Panel*. Or open the *AF3030_sfp.exe* file: this is in the *C:\VXIPNP|WinNT\af3030* directory on a Windows 2000 machine, for example. The soft front panel, similar to that in Fig. 3-2, is displayed.

Detailed help information

Soft front panel controls are all available as driver export functions unless noted otherwise, and are documented in the help files. This operating manual provides an overview of the facilities that the module provides and summarizes its operation; however, refer to the help files for detailed descriptions of functions, together with their parameter lists and return values.

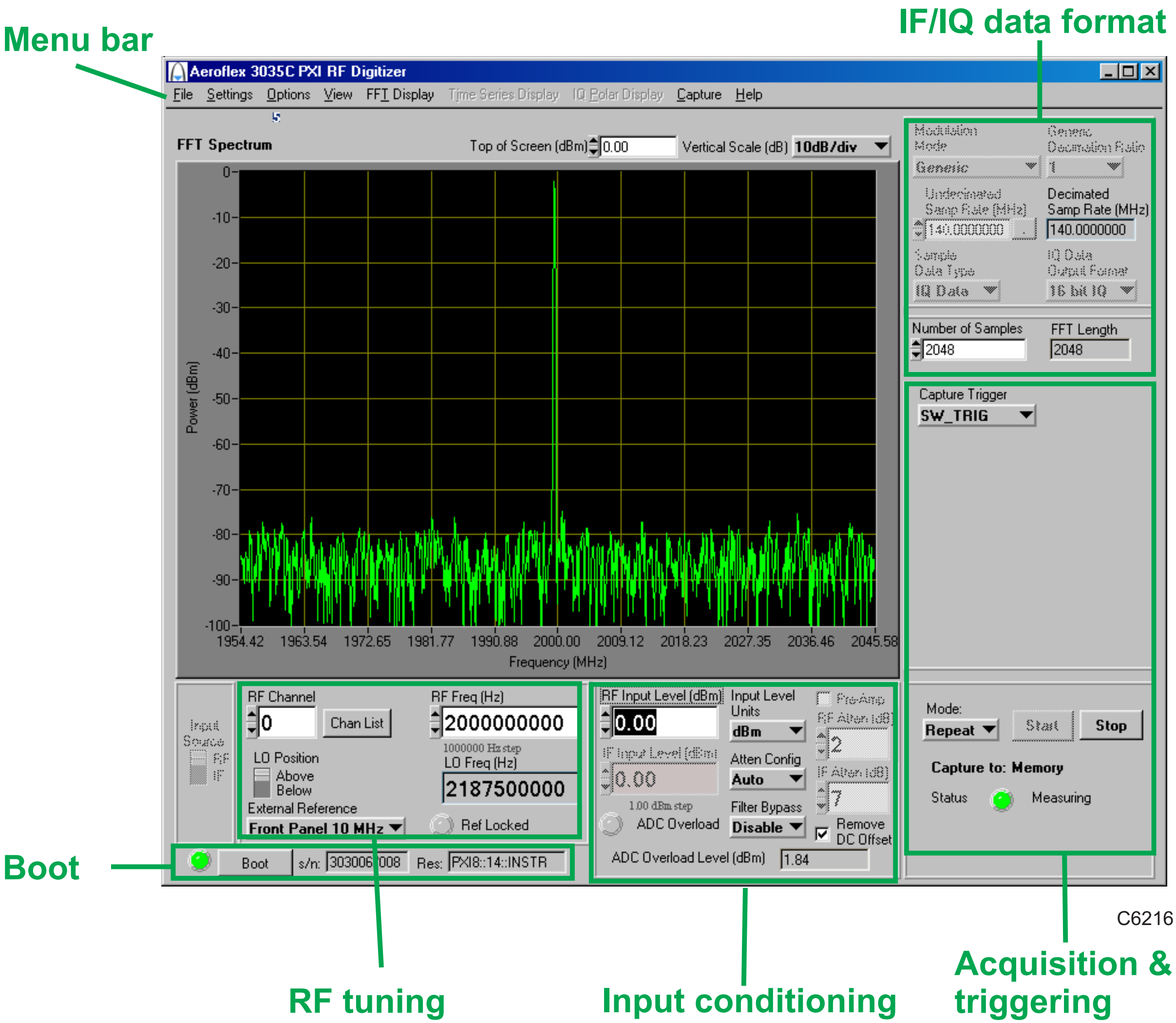


Fig. 3-2 3035C soft front panel

Soft front panel controls

Menu bar

File

Save Captured Data (as ASCII file)… captures the 16-bit sample data into the specified ASCII file.

Save Captured Data (as Binary file)… captures the 16-bit sample data into the specified binary file.

Click **Exit** to close the application.

Settings

Load and **Save** allow you to load and save soft front panel configurations from and to your preferred locations. If you did not change the default location when installing the software, it is *C:\VXIPNP\WinNT\af3030\settings*, and configurations are saved as *.ini* files.

> You can edit, copy and paste settings files as required; for example, you may want to save only a new routing setup without changing other parameters. Edit the saved *.ini* file using a text editor (for example, Notepad) to remove unwanted parameters. Ensure only that you do not delete the General (VendorID, DeviceID) and Version (Major/Minor) parameters. Save the changed file. When the settings file is next loaded, the configuration of the soft front panel changes to match the parameters remaining in the settings file.

Directories lets you choose the default directory for your front-panel configuration settings.

LVDS allows you to set each LVDS Data, Auxiliary and Marker mode for input, output or tri-state (default) operation.

- Spare 0 is controlled by LVDS Data Mode. To use Spare 0 as a trigger input, set LVDS Data to Input. To use Spare 0 as a trigger output, set LVDS Data to Output.
- To use an auxiliary bit as a trigger input, set LVDS Auxiliary to Input. To use an auxiliary bit as a trigger output, set LVDS Auxiliary to Output.
- To use a marker bit as a trigger input, set LVDS Marker to Input. To use a marker bit as a trigger output, set LVDS Marker to Output.

Timer… allows you to configure the internal timer.

List Mode… allows you to configure list mode settings.

Routing Scenarios allows you to select a predefined routing matrix connection. A tick against the scenario's title shows that it is selected.

Selecting or removing a routing scenario affects only the connections specific to that scenario, and does not change any other routing connections. However, changing the routing matrix connections of any scenario invalidates that scenario.

Routing Matrix displays a matrix that provides interconnection between input and output signals on the PXI backplane bus, the DATA connector and the TRIG input, as shown diagrammatically in Fig. 3-3. This provides great flexibility in how you can route signals between modules.

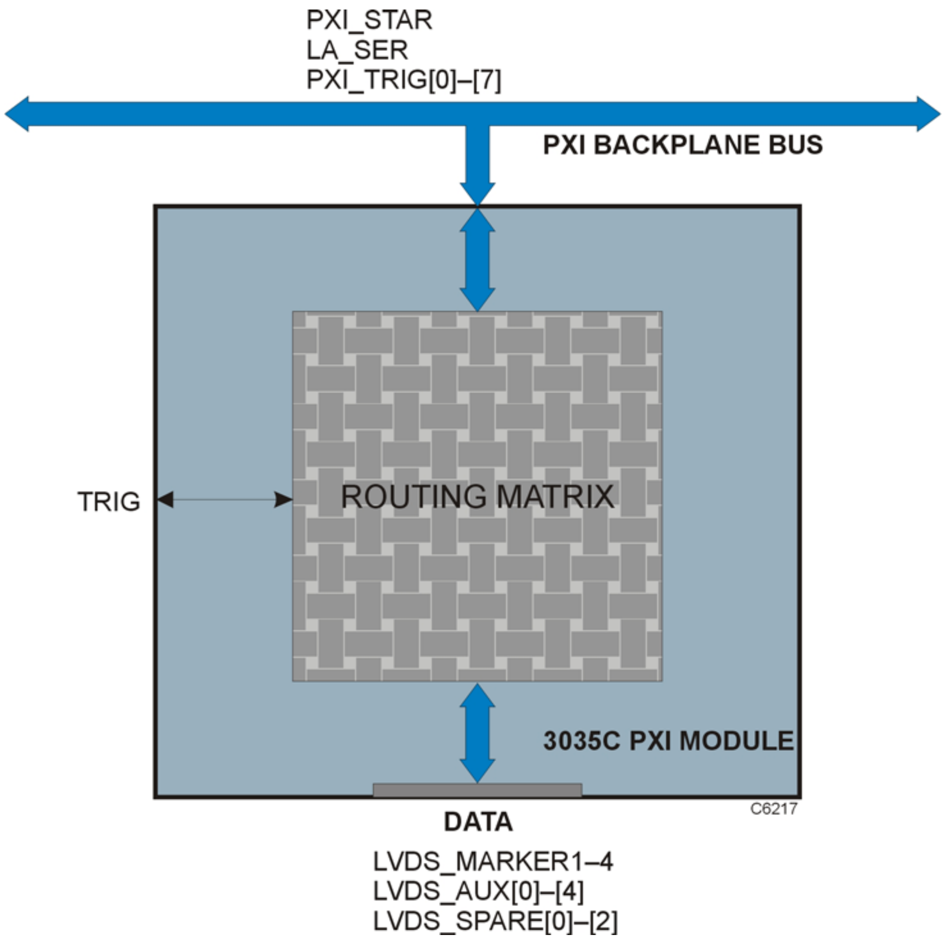


Fig. 3-3 Routing matrix in 3035C

Use the routing matrix (Fig. 3-4) to interconnect signals. Output signals form the body of the matrix. Select appropriate input signals from the drop-down menus under each down-arrow to create the interconnections.

Check the boxes to enable the outputs and select the appropriate LVDS mode.

Reset connects all input signals to GND and disables the outputs (LVDS outputs go tri-state). This is the default state.

When operating the module in default digitizer mode (routing matrix reset), all necessary input, output and trigger signals are available on front-panel DATA, SMA and SMB connectors and there is no need to configure the matrix. If you need to set up particular signal routings, you can define these using the drop-down menus on the matrix and save them using the **Load** and **Save** commands in **Settings**, or use **Routing Scenarios** to access pre-set alternative routings, or contact Aeroflex if you need assistance in defining particular routing requirements.

3035C is a hybrid slot-compatible PXI-1 peripheral module, and so all but one parallel LBL outputs are grayed out and unavailable. Instead, the drop-down menu associated with LBL[6] provides a serial interface LA_SER.

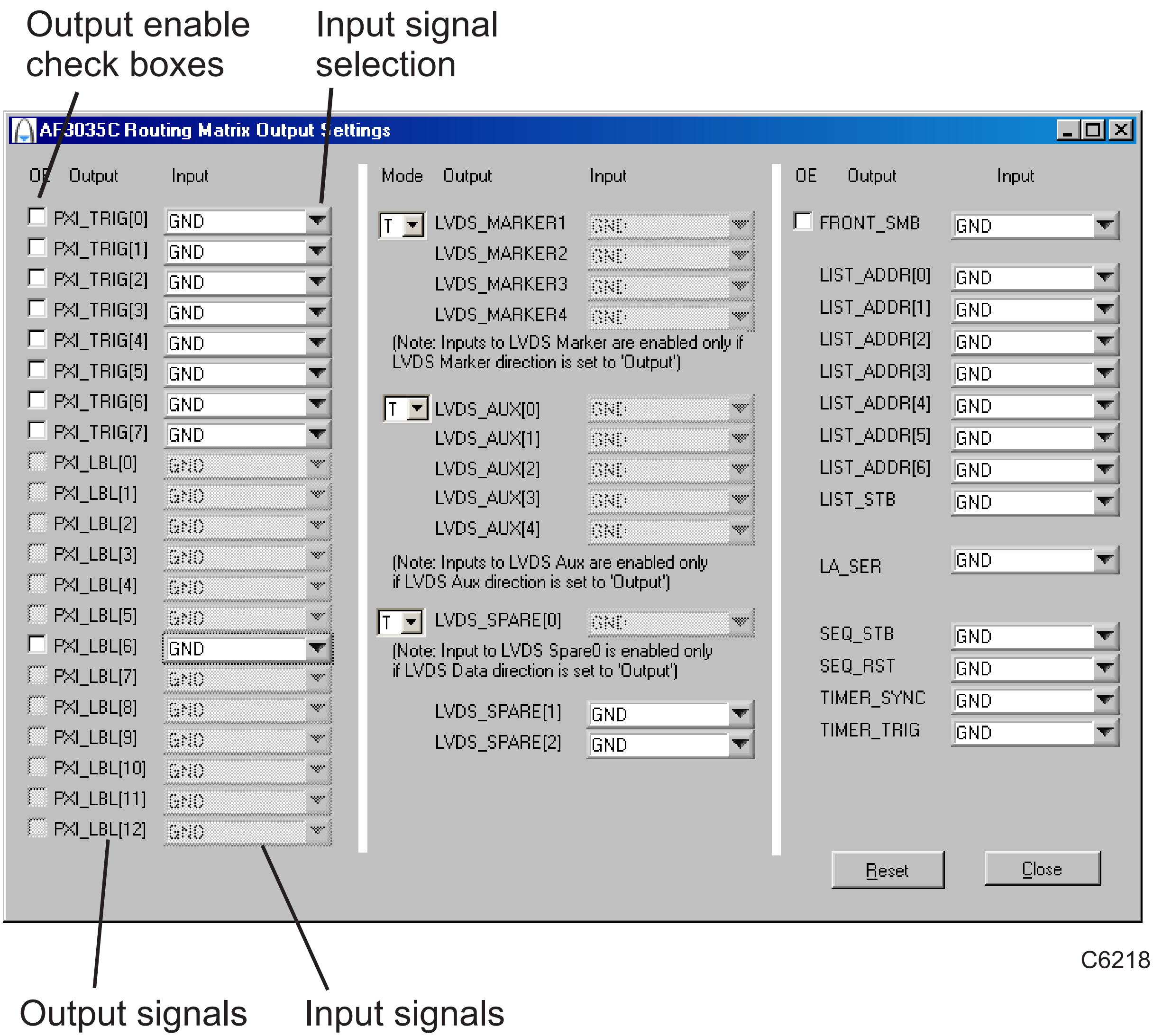


Fig. 3-4 Routing matrix inputs and outputs

Optimization allows you to choose how the module compensates for the effect of temperature changes and RF frequency response.

Auto Temperature Optimization (default) monitors the temperature of the module at regular intervals and adjusts the correction figure for the current temperature. You can turn this off if it might interfere with a time-critical measurement. It is also turned off automatically when List Mode is enabled.

Optimize Temperature Correction forces an immediate update, after which the timer starts a new interval.

Auto Flatness Mode compensates for the slope of the RF response, and may be needed for measurements taken over a wide bandwidth. It applies compensation to ‘flatten’ the response over the chosen bandwidth. The change in RF level due to RF response may not be significant for narrow-bandwidth measurements, which should be taken into account as auto flatness mode compensation may slow measurement time considerably. Default is ‘off’.

Enable Pre-Amp Control, when selected, allows you to switch in the preamp at low signal levels.

Options

Allows you to enable or disable additional instrument options if you have the appropriate password (available from the Aeroflex sales desk). Click **Edit…** to display the options screen (Fig. 3-5).

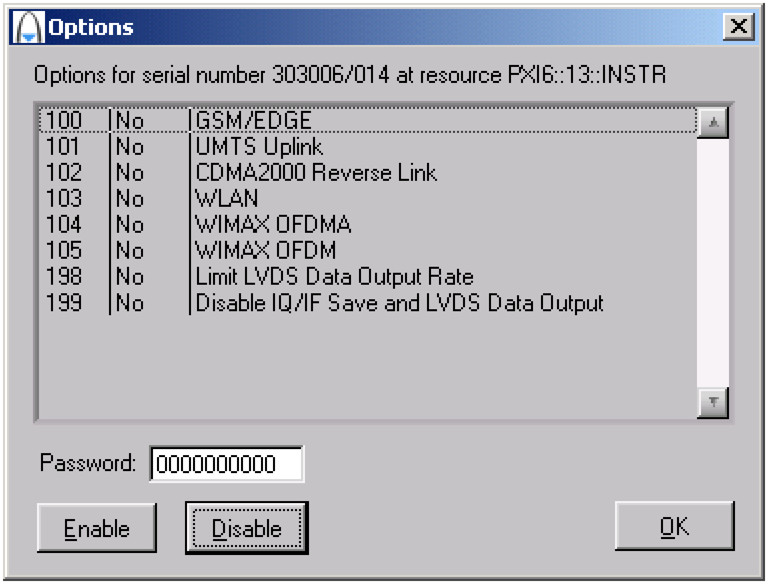


Fig. 3-5 Options screen

Disabled options are shown grayed out. To enable an option, enter the appropriate password. Click **Enable**. The enabled option is shown highlighted in green. Click **OK**.

View

Allows you to view results in different formats.

View FFT (default) displays a single graph showing logarithmic power versus frequency. The default span is 66% of full span. You can modify the top of screen reference power (dBm) and the vertical scaling (dB/div). Select other display settings from FFT Display.

View Time Series displays two graphs showing I and Q magnitude (in IQ mode) or IF magnitude (in IF mode) versus sample number. Sample Start and Sample End let you change the start and stop time of samples, allowing you to 'zoom in' on data. Select other display settings from Time Series Display.

View IQ Polar presents I and Q data as a polar response. Select other display settings from IQ Polar Display.

View Numeric Data displays IQ or IF data that can be placed alongside either the FFT or Time Series views. Numeric data representing the values of I and Q capture data is displayed as I first, followed by Q. Use the scroll bar to inspect long sample records.

FFT Display

This menu is enabled only when View\View FFT is selected. It allows you to hide/display the graticule and save the dB levels of the trace as a *.txt* or other file.

Graticule Visible hides or displays the graticule.

The **Span** menu selects either Full or Truncated (approx. 66%) span. For example, with Modulation Mode set to UMTS and with a Decimation Ratio of 2, Full span is the full decimated bandwidth of the module (30.72 MHz) and Truncated limits this to 20 MHz, placing graticule lines at integer frequencies for easier reading. For Generic Modulation Mode, the Full and Truncated limits are 125 MHz and 81.38 MHz respectively, reflecting the maximum available span of the module with a Decimation Ratio of 2.

Save FFT Trace saves the current FFT trace as a text file. The FFT trace is recorded as an array of dB values. The length of the array is displayed in the FFT Length field. The text file's location is defined in File Setup...

File Setup… allows you to select the filename and location for the FFT trace.

Time Series Display

When **View Time Series** is selected, the Time Series Display menu is enabled, allowing you view I and Q traces on two separate graphs or overlaid in different colors.

Graticule Visible hides or displays the graticule.

IQ Separate Graphs displays separate graphs of Time Series (I) and Time Series (Q). Both graphs are displayed with a common horizontal axis scaling (as set by Sample Start and Sample End).

IQ Overlaid Graph displays colored I and Q traces on a single graph; I is yellow and Q is green.

IQ Power Graph displays the instantaneous magnitude of $\sqrt{I^2 + Q^2}$.

Full Width Sample View adjusts the number of samples displayed in the graph to the number of samples captured.

Y-axis Autoscale: when selected, automatically sets the scaling of signal magnitude to the peak value. When it is deselected, you can set the values manually using the Magnitude Min and Magnitude Max controls above the display. The values of Magnitude Min and Magnitude Max apply to both I and Q when IQ Separate Graphs is selected.

IQ Polar Display

When **View IQ Polar** is selected, the IQ Polar Display menu is enabled, allowing you view I and Q traces on a polar plot.

Graticule Visible hides or displays the graticule.

Autoscale, when selected, scales the I and Q signal magnitudes to the peak value. When it is deselected, you can set the values manually using the IAxis Range (±) and QAxis Range (±) controls above the display.

Capture

By default, the module captures data to the screen (**To Screen Only**), but you can also capture results to ASCII or binary files whilst continuing to display on screen (**To ASCII File and Screen**; **To Binary File and Screen**).

File Setup… opens a browser to define a file extension (default is *.txt*) and location for storing data. Files are saved as interleaved I/Q pairs (I followed by Q) or single IF data, depending on the setting of the Sample Data Type field.

- ASCII IQ file: I and Q values are on new lines, I value followed by Q value.
- Binary IQ file (16-bit mode): I and Q values are stored as 16-bit integers, I value followed by Q value.
  Binary IQ file (32-bit mode): I and Q values are stored as 32-bit integers, I value followed by Q value.

Help

Instrument Information provides the module's PXI resource code and serial number, revision numbers for driver, FPGA and PCI, and its last calibration dates.

About provides the version and date of the soft front panel.

Boot

Click **Boot** to initialize the module and view the Boot Resource window. Resources available for initializing are shown in blue.

Select the 3035C you want to boot.

Boot default FPGA configuration box.
Check this. Do not change the configuration unless you are advised otherwise.

EEPROM caching box.
Ignore for 3035C (has no effect).

Click **OK**. While you select the boot resource, the indicator is amber. Once the module has initialized, the indicator changes to green in a few seconds.

If no calibration data is available, the driver returns a caution. If this happens, return the module for calibration.

s/n:

After the module initializes, this field displays its serial number.

Res:

After the module initializes, this field displays its VISA resource string.

RF tuning

RF Channel

Sets the currently active channel in a range of 0 to 127.

Chan List

Click this to set up the channels for list mode operation. You can Load and Save the settings file to make setup easier.

RF Freq (Hz)

This is the RF input frequency. This defines the center frequency of the FFT trace and selects appropriate correction values.

The module is tuned by setting the RF frequency and the LO offset direction (above or below). From these two values, the module calculates the LO frequency that must be applied to the LO input.

Set the input frequency using the up/down arrows or by entering the frequency in Hz or scientific (e) notation, in the range 250 kHz to 6.0 GHz.

LO Position

Displays the local oscillator position relative to the RF frequency.

Set to Above to make the LO higher than the RF, and to Below to make the LO lower than the RF. For some frequencies, LO Position is fixed and cannot be changed.

LO Freq

Shows the frequency to which a 3010 Series RF synthesizer module or other source should be set in order to provide the correct LO frequency for the 3035C. If you are using a 3010 Series module, simply double-click on the field, copy the value, and paste it into the RF Frequency (Hz) field on the 3010 Series module's soft front panel.

External Reference

Lock to 10MHz causes the ADC clock to lock to the 10 MHz reference connected to the 10 MHz I/O connector. **Free Run** allows internal oscillators to run at indeterminate frequencies. **PCI Backplane** causes the ADC clock to lock to the 10 MHz reference from the PCI backplane.

Input conditioning

RF Input Level (dBm)

Set this to the peak level of the input RF signal to insure the best dynamic range and signal-to-noise ratio.

Set the RF input level using the up/down arrows or by entering the level, in the range −99.00 to +30.00 dBm in Auto Atten Config mode. In Auto IF or Manual Atten Config mode, this value is not used but the maximum value is capped to +20 dBm.

RF Atten

Sets the RF attenuator value, which changes the input level to the mixer. This value can only be adjusted manually if Atten Config is set to Manual or Auto IF.

Set the RF attenuator level using the up/down arrows or by entering the level, in the range 0 to +31 dB, in 1 dB steps.

IF Atten

Sets the IF attenuator value, which changes the input level to the ADC. This value can only be adjusted manually if Atten Config is set to Manual.

Set the IF attenuator level using the up/down arrows or by entering the level, in the range 0 to +62 dB in 1 dB steps (you are unlikely to use more than +31 dB).

Input Level Dimensions

Establishes the measurement units as dBm, dBμV, dBmV, dBV, V or mW.

Atten Config

Auto	the RF input level set is used to optimize RF and IF attenuator gain settings automatically.
Auto IF	you have manual control of RF attenuation and preamp but the IF attenuator setting is automatically set by the driver.
Manual	you have complete control over the settings of the RF and IF attenuators and preamp; the driver ignores the set RF input level.

Filter Bypass

When enabled, causes the anti-aliasing filter to be bypassed, allowing signals outside its passband to reach the ADC. Level calibration is maintained. Allows you to observe spurii and other signals within the module's bandwidth that would otherwise be removed by the filter.

ADC Overload (LED)

Indication is red if the ADC was overloaded during the last acquisition.

ADC Overload Level

Indicates the RF input level that could cause ADC Overload error. The displayed overload level is clamped to the safe input level.

Pre-Amp

When Atten Config is set to Auto IF or Manual, ticking this box switches in the preamp. In Auto mode, the preamp is switched in automatically when signal levels require it. Disable the preamp to allow faster switching when operating in List Mode.

Remove DC Offset

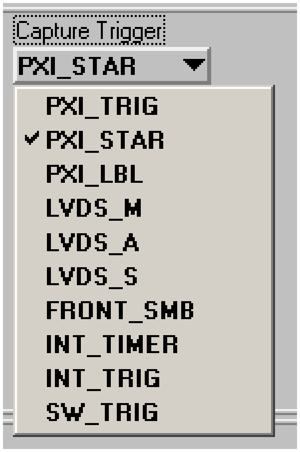
Removes the DC component from captured IF or IQ data. Removes DC components at the edge of the span at full and/or ½ sample rate.

Note*: if no signal is present on the input, a sawtooth waveform is displayed on I and Q time series screens, due to a DC component introduced internally by the ADC transfer function.*

Acquisition & triggering

Capture Trigger

Allows you to select the trigger source from a drop-down list:



Software trigger

- **SW_TRIG**
  This is a non-triggered capture mode. Click on **Start** to capture samples (defined by Number of Samples) when in Single/Repeat mode, without waiting for any external event. Click **Stop** to end the capture.

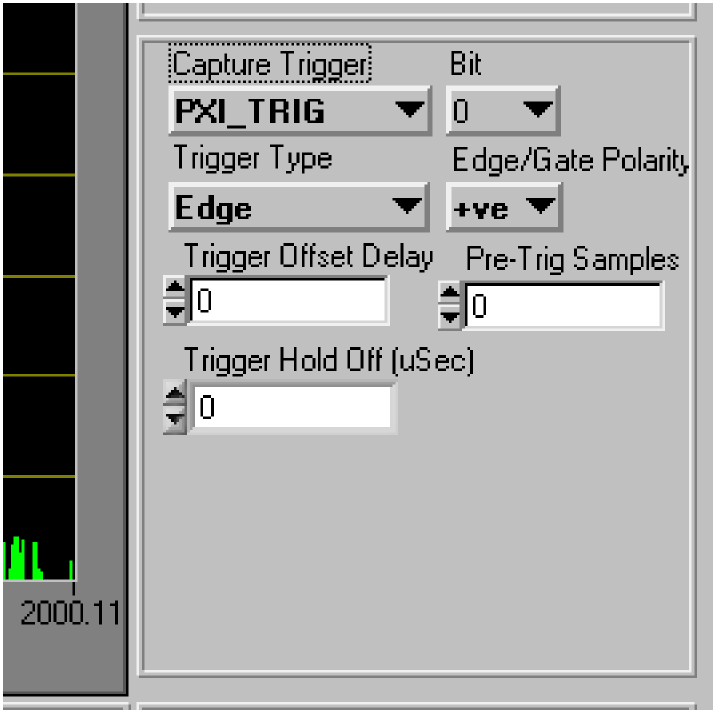
Hardware triggers

Remaining triggers on the drop-down list are hardware triggers. When any of these is selected, triggering is dependent on trigger events, including the correct arming of the trigger.

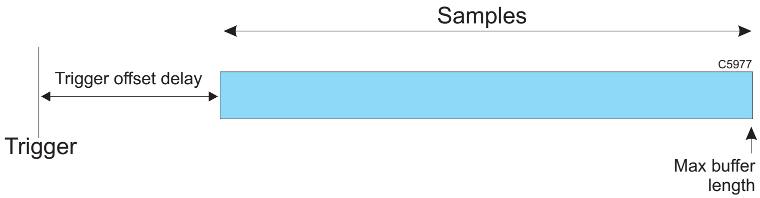
The module ignores triggers that occur during the sample capture.

Refer to the help files for full details.

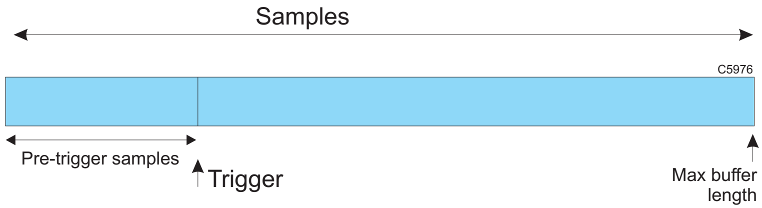
Most of the hardware triggers share a common triggering interface:



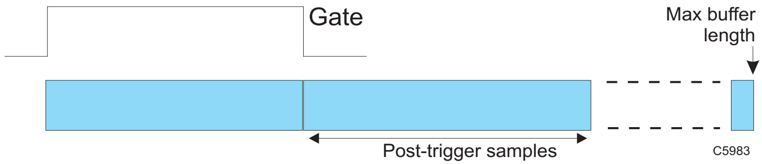
Trigger Type	Set to Edge or Gate
Edge/Gate Polarity	Set +ve or –ve
Trigger Offset Delay	Delays the trigger by a specified number of output sample periods.



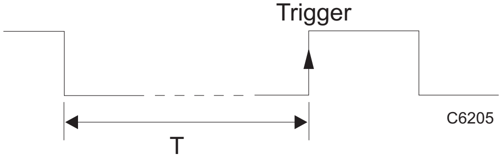
Pre-Trig Samples (Edge trigger type)	Sets the number of pre-trigger samples present in the captured data buffer. Increase this value to move the position of the trigger point in the captured data further from the start.



Post-Trig Samples (Gate trigger type)	Sets the number of post-trigger samples present in the captured data buffer.

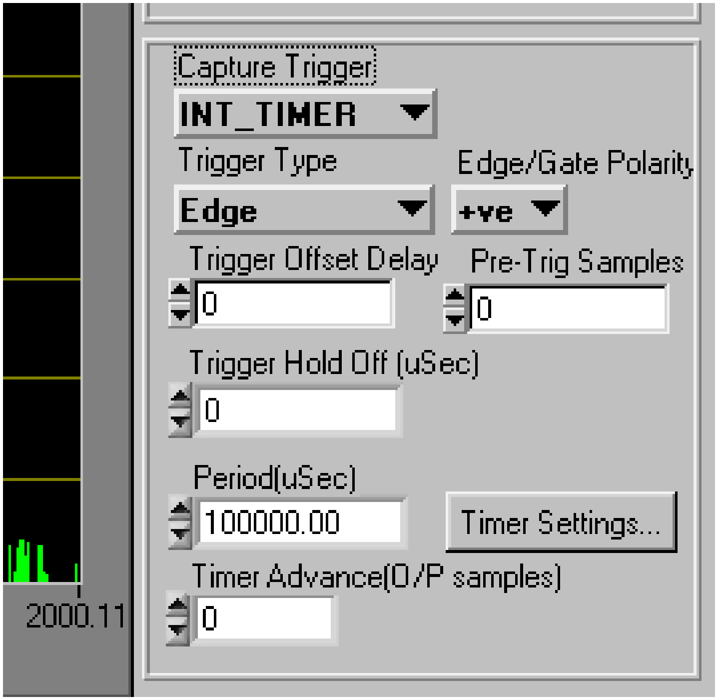


Trigger Hold-Off — The trigger signal is valid only if the inactive period T before the active edge of the signal is greater than the specified trigger hold-off period.



- **PXI_TRIG** [0–7]
  Takes its trigger input from any one of 8 bits of the PXI trigger bus that is common to all modules in the chassis.
- **PXI_STAR**
  Takes its trigger input from a module that has ST functionality and is fitted in PXI slot 2.
- **PXI_LBL** (Local Bus Left) [6]
  Takes its trigger input from the slot to the left of the 3035C (viewed from the front panel), using the PXI local bus. This bit is common only to the 3035C and the module to its left.
- **LVDS_M** [1–4]
  Takes its trigger from any of four Marker bits on the DATA connector. Ensure that Settings/LVDS/Marker Mode is set to Input.
- **LVDS_A** [0–4]
  Takes its trigger from any of five Auxiliary input bits on the DATA connector. Ensure that Settings/LVDS/Auxiliary Mode is set to Input.
- **LVDS_S**
  Takes its trigger from the Spare 0 input bit on the LVDS data bus. Ensure that Settings/LVDS/Data Mode is set to Input. Because the data bus is set to receive when this trigger is used, it is not then possible to output data on the DATA connector.
- **FRONT_SMB**
  Takes its trigger from the TRIG connector on the module's front panel.

- **INT_TIMER**
  Takes its trigger from the internal timer. This timer trigger can also be routed to other modules using the routing matrix. Similarly, this timer can be synchronized with the external signal connected to the TIMER_SYNC signal in the routing matrix.



Click **Timer Settings…** to display the Timer Settings screen (Fig. 3-6).

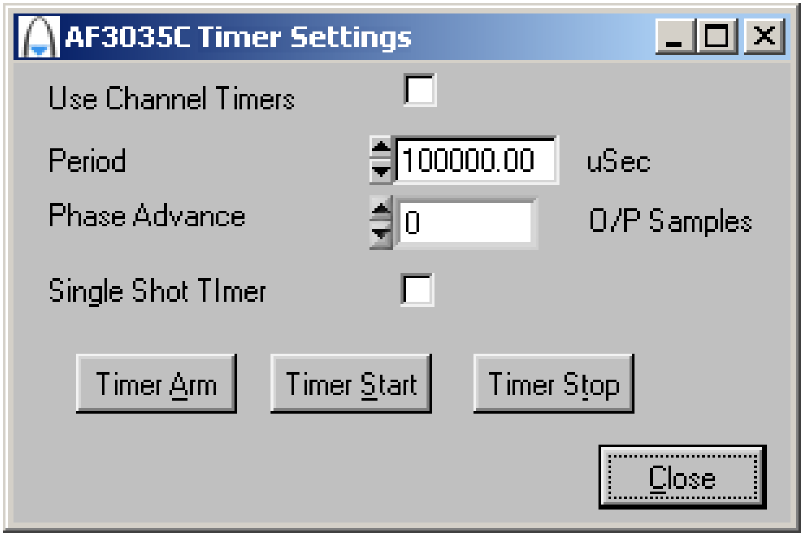


Fig. 3-6 Timer settings

Use Channel Timers — when checked, lets you use a different timer period for each channel. The timer period is determined by the active channel's Period (see below), and applies while that channel is active. This mode is useful in setting up variable dwell list mode.

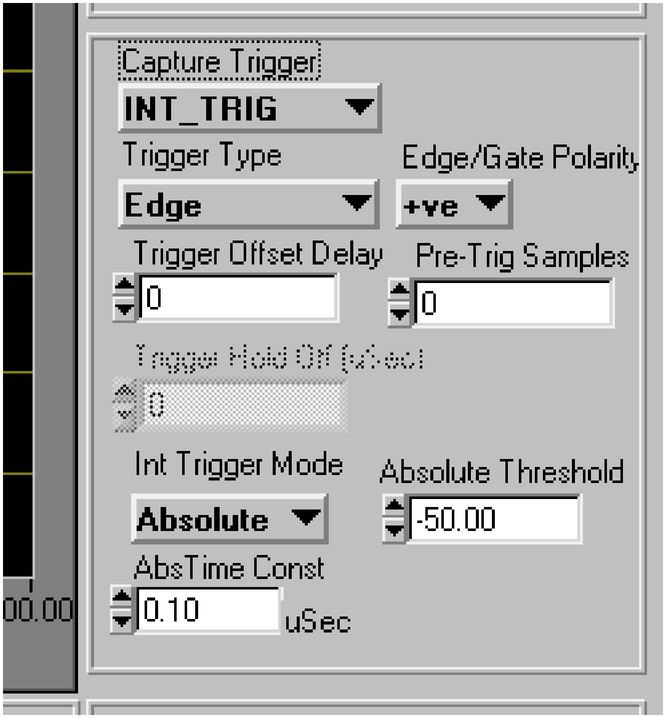
The channel timer period is measured in number of output samples, so changes if the sample rate changes. When the channel changes, the timer restarts, using the period set for that channel.

If Use Channel Timers is disabled, the timer period becomes the common timer period, specified in μs. This timer period stays the same irrespective of which channel is active, and does not restart when the channel changes.

Period	Sets the period of the active channel (in number of output samples) if Use Channel Timers is enabled. Otherwise, sets the common timer period in µs. Mark/space ratio in either mode is 50%.
Phase Advance	Adjusts the phase of the internal timer signal in multiples of the output sample clock period. Allows you to synchronize the timer trigger with an external signal. Not available if Use Channel Timers is enabled.
Timer Arm	Arms the timer so that an external signal connected to TIMER_TRIG in the routing matrix triggers the timer (rising edge).
Timer Start	Starts the timer if it was stopped, otherwise ignored if the timer is already running. Initial state of timer is ‘High’.
Timer Stop	Stops the timer if it is running, and disarms the timer trigger. Once the timer is stopped, an external signal cannot start it without re-arming it.

Settings for Period and Phase Advance (in common timer mode only) appear on the front panel as well as on the Timer Settings screen.

- **INT_TRIG**
  Takes its trigger from the internal level trigger.



Int Trigger Mode	Select the internal level trigger mode: Absolute/Relative Absolute: the digitized signal is filtered using an absolute time constant. An internal level trigger is generated when the level of this filtered signal exceeds the absolute level trigger threshold (specified in dBm). The absolute time constant and level settings may affect the trigger delay. Relative: the digitized signal is filtered using both a fast and a slow time constant. For a step level change, the amplitude difference between the two resultant filtered signals produces a pulse, its duration and level determined by the difference between the fast and slow time constants. The pulse is then compared with the 'relative threshold trigger level' to create the internal trigger. Fig. 3-7 shows this. When the relative threshold trigger level is entered as positive, the difference signal = (fast signal – slow signal). When relative threshold trigger level is entered as negative, the difference signal = (slow signal – fast signal). Only +ve Trigger Edge/Gate Polarity is available when using relative mode.
AbsTime Const	Sets the time constant for the absolute level internal trigger.
Absolute Threshold	Sets the absolute threshold level in dB.
Slow/Fast Time Const	Sets the slow and fast time constants used in relative internal trigger mode.
Relative Threshold	The threshold value (dBm) compared with the difference signal filtered using Relative Slow and Fast Time Constants.

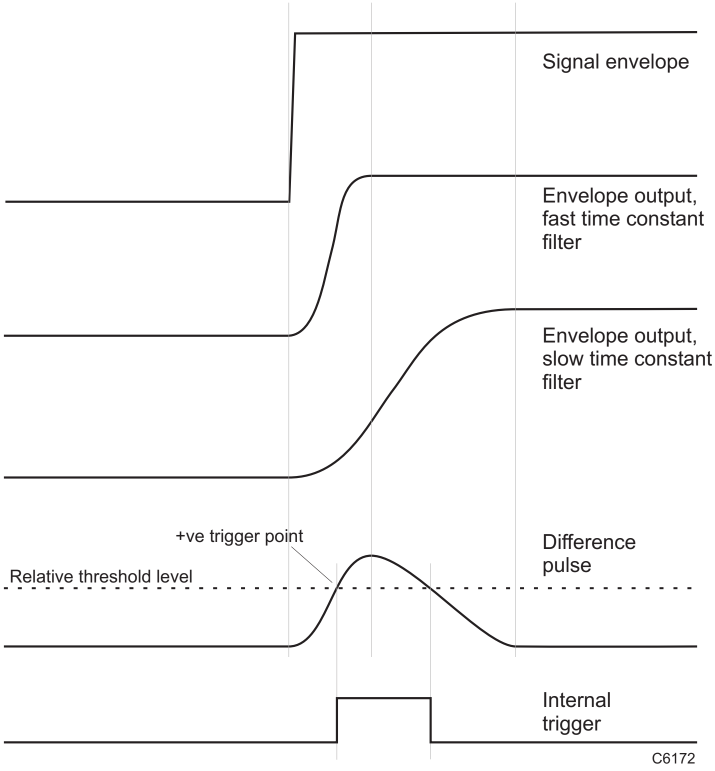


Fig. 3-7 Relative internal level trigger mode

Trigger mode and control

Mode:

Selects **Single**-shot or **Repeat** data capture.

Use with the **Start** and **Stop** buttons to initiate and stop data capture.

The indicator shows the status of the trigger or capture: green when waiting for a trigger or capturing, gray when idle.

IF/IQ data format

Sample Data Type

Select IQ or IF sample data type.

- IQ Sample Data: output sample rate is determined by the Modulation Mode and Decimation Ratio
- IF Sample Data: output sample rate is fixed at 250 MHz.

Modulation Mode

(IQ data format only) Sets the digital modulation mode. Select from Generic, UMTS, GSM, CDMA2000 1X or 2319 Emulation.

The sample rate varies, depending upon modulation mode and decimation ratio:

- Generic: user-defined. Use this mode to create or emulate any modulation scheme.

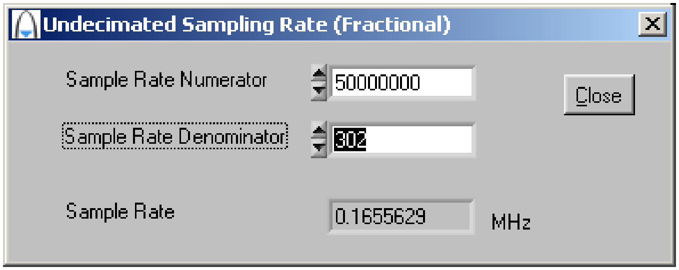
  Enter any Undecimated Sample Rate in the range 7630 Hz to 250 MHz (PCI transfer) (62.5 MHz LVDS 16-bit IQ data transfer or 31.25 MHz 32-bit IQ data transfer) with a Generic Decimation Ratio of 1.

  Alternatively, enter a different Generic Decimation Ratio and scale the Undecimated Sample Rate accordingly.

  The resultant sample rate is shown in the Decimated Sample Rate box.

  or

  define a fractional rate by setting the numerator and denominator. Click on the button adjoining the Undecimated Sample Rate box to open the popup panel and enter a fractional sample rate:



Pre-defined rates:

- UMTS data mode: 61.44 MHz/2^N (where N = 1 to 10)
- GSM resampled IQ data mode: 13 MHz/(3 * 2^N), where N = 0 to 4 ($2^{(4-N)}$ times symbol rate of 13 MHz/48)
- CDMA2000 1X resampled IQ data mode: 9.8304/2^N, where N = 0 to 3 ($2^{(3-N)}$ times chip rate of 1.2288 MHz)
- 2319 emulation mode: 65.28/2^N, where N = 4 or 5.

Decimation Ratio (Generic/GSM/UMTS/CDMA2000 X1/2319E)

(IQ data format only) Select a decimation ratio, dependent on the modulation mode:

GENERIC	2^n where n = 0 to 14 (max)
GSM	2^n where n = 0 to 4
UMTS	2^n where n = 1 to 10
CDMA2000 1X	2^n where n = 0 to 3
2319E emulation	2^n where n = 4, 5

See Data timing.

Undecimated Samp Rate (MHz)

Displays the internal undecimated sampling rate before division by the decimation ratio.

GENERIC	250 MHz	
UMTS	61.44 MHz	= 3.84 MHz (3GPP chip rate) x 16
GSM	4.3333 (rec.) MHz	= 270.8333 (rec.) kHz (GSM bit rate) x 16
CDMA2000 1X	9.8304 MHz	= 1.2288 MHz (CDMA2000 chip rate) x 8
2319E	65.28 MHz	= 3.84 MHz (3GPP chip rate) x 17
IF	250 MHz	

IQ Data Output Format

Select 16- or 32-bit, subject to the modulation mode and decimation ratio chosen.

Sample rates

Modulation	Decimation ratio	IQ sample rate (Msymbol/s)	IQ data format
GENERIC	2^n where n = 0 to 14 (max)	variable	6 (when Output Sample Rate > 31.25 MHz) 16/32 (when Output Sample Rate ≤ 31.25 MHz)
UMTS	2	30.72	16/32
	4	15.36	16/32
	8	7.68	16/32
	16	3.84	16/32
	32	1.92	16/32
	64	0.96	16/32
	128	0.48	16/32
	256	0.24	16/32
	512	0.12	16/32
	1024	0.06	16/32
GSM	1	4.33333	16/32
	2	2.16666	16/32
	4	1.08333	16/32
	8	0.541667	16/32
	16	0.270833	16/32
CDMA2000	1	9.8304	16/32
	2	4.9152	16/32
	4	2.4576	16/32
	8	1.2288	16/32
2319E	16	4.08	16/32
	32	2.04	16/32

Decimated Samp Rate (MHz)

Displays the result of the undecimated sampling rate divided by the decimation ratio.

Number of (IF/IQ) Samples

The name of the field changes to reflect the sample type selected.

Sets the sample size (number of samples to be captured):

> 3035C: up to 64M IQ pairs with 32-bit storage, 128M IQ pairs with 16-bit storage, or 256 IF samples.

FFT Length

Varies with number of IF/IQ samples set. Minimum 16, maximum 2048.

List mode operation

Introduction

List mode operation associates a list address with a particular RF setup (channels 0–127). When the module is set to list mode operation, a new address, when strobed in, causes the module to change to the RF setup (channel) associated with that address.

List mode operation facilitates fast channel hopping during, for example, testing of transmitter/receiver modules where numerous different RF level and frequency settings are needed. A seven-bit list address selects the channel. A strobe signal, internally or externally generated, then causes the instrument to switch between channels as required. Flexibility is provided to allow channel hopping using a variety of control sources.

List addresses for list mode operation can be provided manually, or from an external source via the signal routing matrix (providing access to backplane bus, LVDS and other address sources), or from an internal sequential counter. The strobe signal that changes the list address can be sourced externally via the routing matrix, or internally.

Channel List

Click **Chan List** on the soft front panel to display individual channel list settings (Fig. 3-8). This is where you define channel setup for list mode operation.

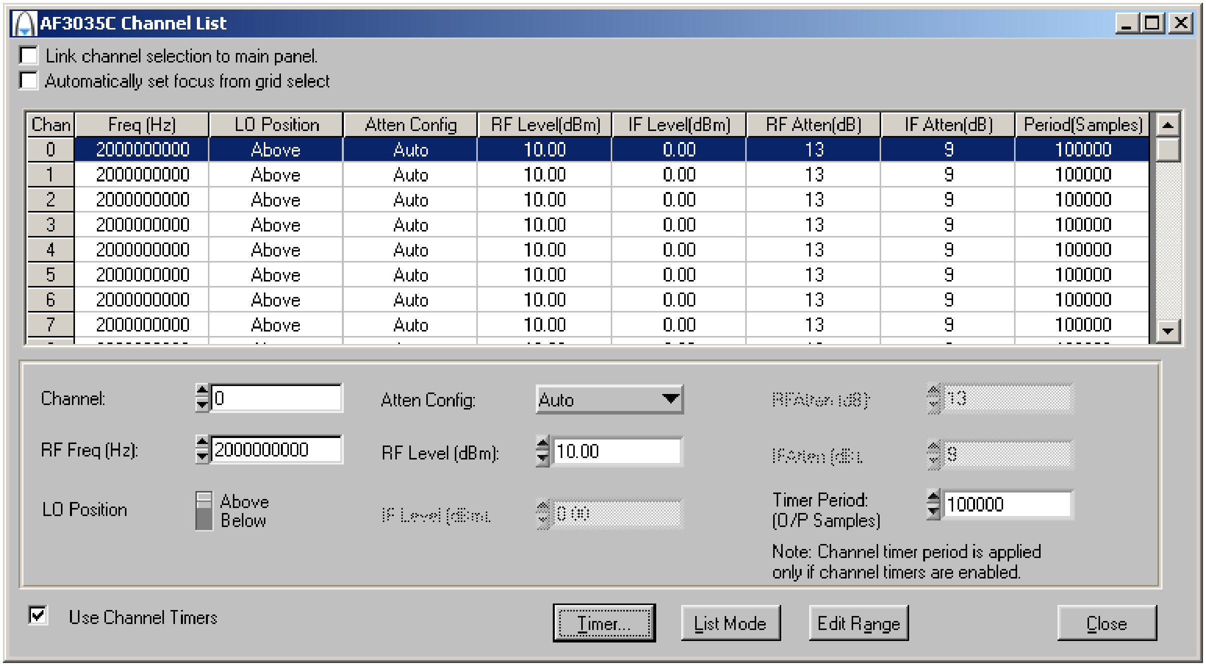


Fig. 3-8 Edit channel list settings

Edit individual channel parameters by selecting the specific channel. Channel parameters are:

Freq (Hz)
LO Position
Atten Config
RF Level (dBm)
RF Atten (dB)
IF Atten (dB)
Period (µs/output samples

Select the channel to be edited either by changing the channel number on the panel or by clicking on the corresponding channel row in the channel list.

If you check the **Link channel selection to main panel** box, changing the channel number on this panel makes it become the active channel on the soft front panel.

Check the **Automatically set focus from grid select** box to make the associated channel parameter field active when you click on a channel parameter in the grid.

Check the **Use Channel Timers** box to use the active channel's period as the timer period for that channel. If the box is unchecked, the common timer period (measured in µs) applies to all channels. See Timer Settings.

Click **Timer…** to display the Timer Settings screen.

Click **Edit Range** to display the Edit Channel Range screen (Fig. 3-9), which lets you apply changes to a set of channels simultaneously, speeding up channel setup.

Define start and finish values for address numbers in the **Chan range, from:** and **to:** fields.

Insert values and click **Set** for each field. You are asked to confirm each action. When finished, click **Close** to return to the Channel List screen.

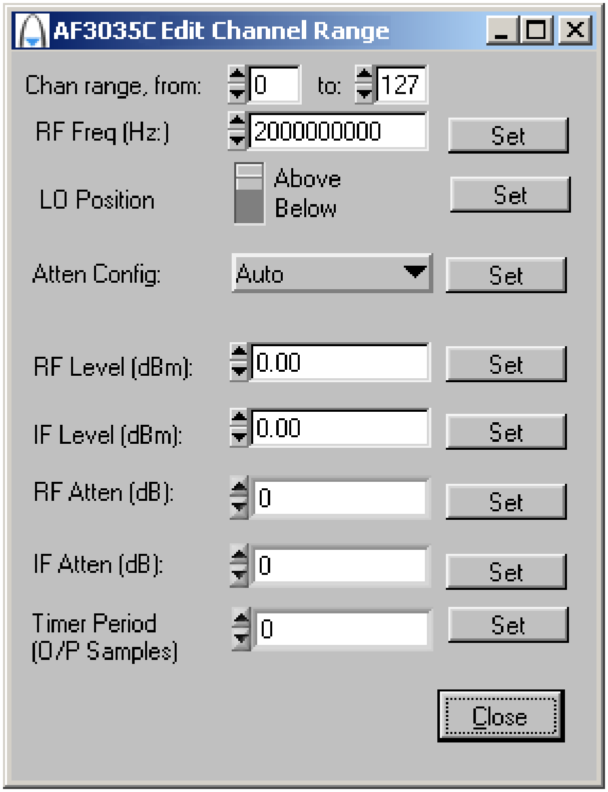


Fig. 3-9 Edit all channel settings

Click **List Mode** to display the List Mode Settings screen, which lets you set up addressing and strobing, and the internal counter.

List Mode Settings

Click **List Mode** on the Channel List screen to display the List Mode Settings screen. From here, you can define the list address source, and how the strobe (internal or external) that actions a new list address is handled. You can also set up the internal sequential counter and the timer that drives it.

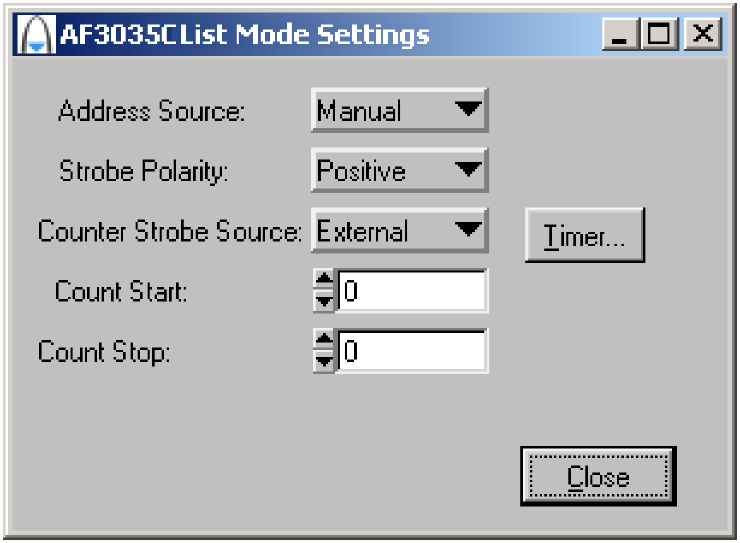


Fig. 3-10 Edit list mode settings

Address Source

Defines the source from which the seven-bit-wide list address is obtained.

Manual: RF list addresses are register-driven values, manually controlled by setting the **RF Channel**.

External: RF list addresses are sourced from the signal routing matrix (Fig. 3-4) on the strobe signal connected to LIST_STB.

Counter: RF list addresses are sourced from the internal sequential counter.

Strobe Polarity

Defines whether a positive- or negative-going edge is active for the strobe signal.

Counter Strobe Source

Defines the method used to sequence the internal List Counter register, when Address Source is set to Counter. When sequenced, the resulting change of address (the count value) automatically causes an internal strobe signal to be generated, which actions the new list address.

External: an external strobe, sourced from the signal routing matrix (Fig. 3-3), causes the counter to count up or down, providing a new list address.

Timer: the counter strobe signal is generated periodically by an internal timer, whose period is set by Timer Dwell.

Counter Start

Defines the start address of the list counter. If this value is less than the value of Counter Stop, the counter increments; otherwise it decrements. Setting this value also resets the list count to the next start address.

Counter Stop

Defines the stop address of the list counter. If this value is greater than the value of Counter Start, the counter increments; otherwise it decrements. Setting this value also resets the list count to the next start address.

Timer Dwell

Defines the period of the list timer, in units of 0.1 μs. The range is 1 μs to 600 s.

Timer…

Click to display the Timer Settings screen.

Driver export functions

On-line help and functional documentation for driver export functions are available on the CD-ROM supplied with your module. They are installed onto your computer at the same time as the drivers.

Driver installation folder

Find help and functional documentation in the driver installation folder on your computer. This is typically:

C:\vxipnp\winnt\af3030

Help

Within the driver installation folder are help files that provide detailed descriptions, parameter lists and return values for all available functions. Help files are provided in three formats:

af3030.doc	3030 Series function documentation	Text file
af3030.hlp	3030 Series Visual BASIC function reference	Windows Help file format
af3030_C.hlp	3030 Series C language function reference	Windows Help file format

We recommend that you use the C or Visual Basic formats, as these are easier to navigate.

The file opens at the Contents page:

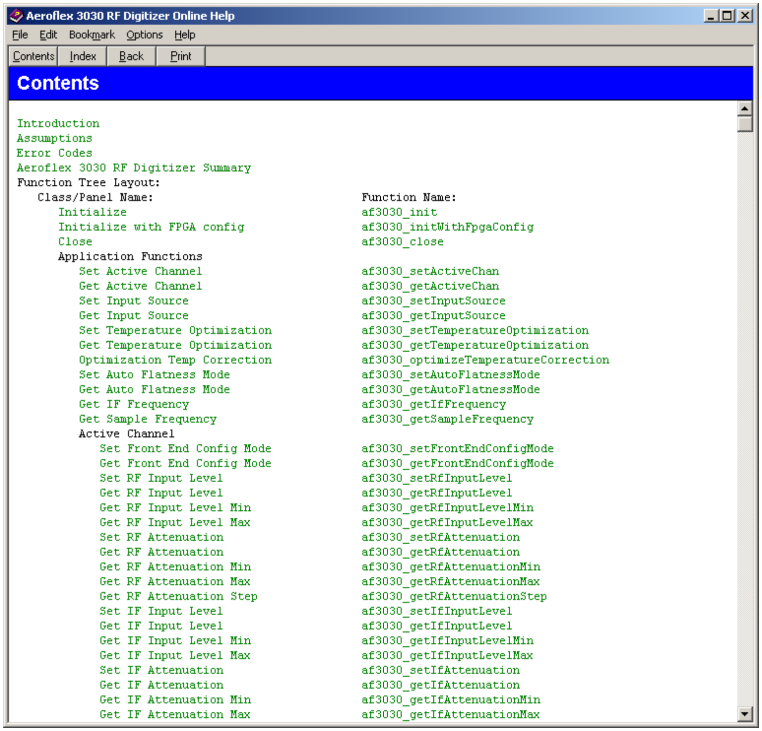


Fig. 3-11 Online help contents — example

Hyperlinks from here take you to

- Introduction
- Assumptions
- Error codes
- Functions listings

Functions listings

Functions are grouped by type. Click on the hyperlink for details of the function. Each function has a description of its purpose, and may have a list of parameters and return values.

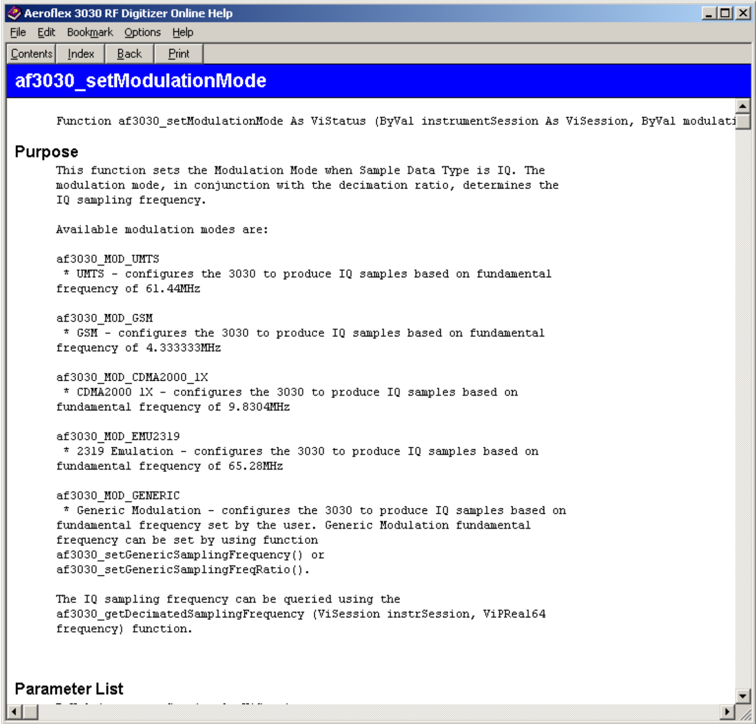


Fig. 3-12 Function description — example

RF digitizer using 3010 Series and 3035C

Refer to *3000 Series PXI Modules Installation Guide for Chassis* (part no. 46882/667) and *PXI Studio User Guide* (part no. 46892/809), both supplied on the CD-ROM with the module, for detailed information on creating a fully functional RF digitizer using the 3035C and 3010 Series modules together. The afDigitizer dlls and PXI Studio application combine the functions of the individual modules to provide a single interface with the appearance and functionality of an integrated instrument.

Appendix A
DATA connector and timing

The DATA connector is a 68-way female VHDCI-type LVDS (low-voltage differential signaling) interface. It can be used to output data and associated control and timing signals.

The DATA connector is shown in Fig. A-1. LVDS data conforms to ANSI/TIA/EIA-644.

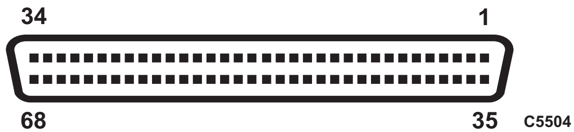


Fig. A-1 DATA connector (looking onto front panel)

The DATA interface provides:

- output of IF or IQ data
- input/output of triggering, List Mode and Timer signals.
- clock.

The electrical level is LVDS: V_{OH} typically 1.38 V, V_{OL} typically 1.03 V

Table A-1 DATA pin-out

Contact	Function	Contact	Function
1	AUX0-	35	AUX0+
2	AUX1–	36	AUX1+
3	AUX2–	37	AUX2+
4	SPARE1–	38	SPARE1+
5	SPARE2–	39	SPARE2+
6	CLK_IN–	40	CLK_IN+
7	GND	41	GND
8	CLK_OUT–	42	CLK_OUT+
9	D0–	43	D0+
10	D1–	44	D1+
11	D2–	45	D2+
12	D3–	46	D3+
13	D4–	47	D4+
14	D5–	48	D5+
15	D6–	49	D6+
16	D7–	50	D7+
17	D8–	51	D8+
18	D9–	52	D9+
19	D10–	53	D10+
20	D11–	54	D11+
21	D12–	55	D12+
22	D13–	56	D13+
23	D14–	57	D14+
24	D15–	58	D15+
25	IQSELECT_OUT–	59	IQSELECT_OUT+
26	IQSELECT_IN–	60	I/QSELECT_IN+
27	SPARE0–	61	SPARE0+
28	GND	62	GND
29	MARKER1–	63	MARKER1+
30	MARKER2–	64	MARKER2+
31	MARKER3–	65	MARKER3+
32	MARKER4–	66	MARKER4+
33	AUX3–	67	AUX3+
34	AUX4–	68	AUX4+

Data format

The data output to the DATA interface is real-time. In resample mode, data is output using a 250 MHz clock (but bursted to achieve the correct average sample rate).

D0-D15 (Sample DATA) in Output Mode	Sample Data Output Format: 16-bit IQ: 2 x D[15:0], I followed by Q, D[0]=LSB. 32-bit IQ: 4 x D[15:0] in order I MSW, I LSW, Q MSW, Q LSW, D[0]=LSB.
IQSELECT_OUT	Specifies content of D0-D15 in output mode when sample data format is IQ. IQSELECT=1 for rising CLK_OUT indicated I data on D0-D15. First IQSELECT transition to '0' from '1' on the rising edge of CLK_OUT indicates **start** of the Q data. In 16-bit mode, Q data is valid for one clock whereas in 32-bit mode, Q data is valid for two clocks after IQSELECT changes to 0. Note that IQSELECT stays 0 even if Q data is transferred. Thereafter, Q is indeterminate until IQSELECT_OUT goes positive to define a new IQ pair. IQSELECT_OUT stays =0 at all times in IF mode.
CLK_OUT	Output clock signal.

Data timing

Data transmission for generic modulation mode

In this mode, IQ data is resampled to produce IQ data in the range 125 MHz/2^N where N = 0 to 13. Example timing relationships between data rate and clock frequency for the DATA interface are shown in Fig. A-2 and Fig. A-3. IQSEL_OUT is toggled only when an IQ data pair is being transmitted. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at 125 MHz. Maximum IQ sample rate is 62.5 Ms/s (for 16-bit I&Q) or 31.25 Ms/s (for 32-bit I&Q). In Fig. A-2, it is a non-integer value, and only the Q value occupying the clock period that follows the falling edge of IQSEL_OUT is valid. In Fig. A-3, the chosen decimated data rate of 62.5 Ms/s means that the ratio of clock to data rate is 2.

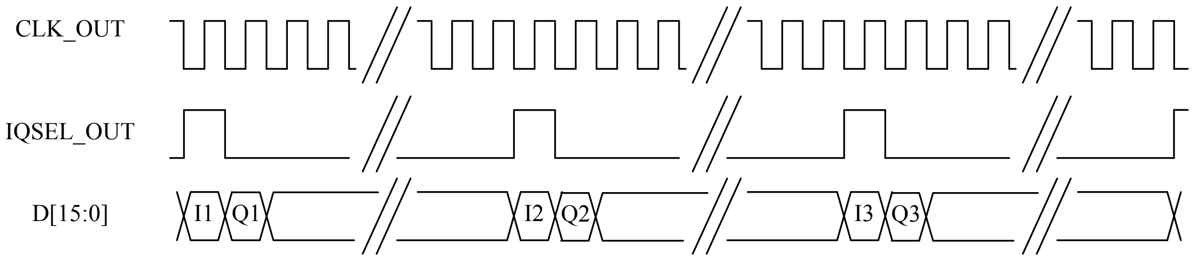


Fig. A-2 DATA timing for generic modulation in 16-bit IQ mode, non-integer relationship

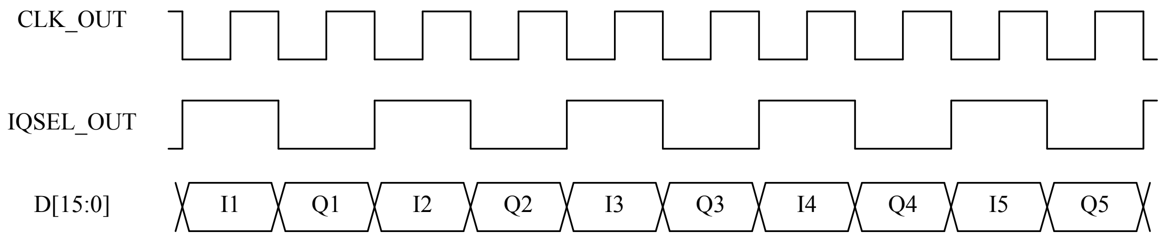


Fig. A-3 DATA timing for generic modulation in 16-bit IQ mode, integer relationship

Data timing for UMTS modulation mode and decimation ratio of 2

The ADC in the module is clocked at a rate of 125 Ms/s. The module's soft front panel allows both the modulation mode and the decimation ratio to be selected. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted. If UMTS is selected as the modulation mode and a decimation rate of two is selected, the IQ data rate is 30.72 Ms/s. The ratio of ADC clock rate to IQ sample rate is $\frac{125\,\text{MHz}}{30.72\,\text{MHz}} = 4.07$, a non-integer value that means that data is output sometimes on the 4th clock pulse and sometimes on the 5th. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. When configured in this way, the timing relationships for the DATA interface are as shown in Fig. A-4.

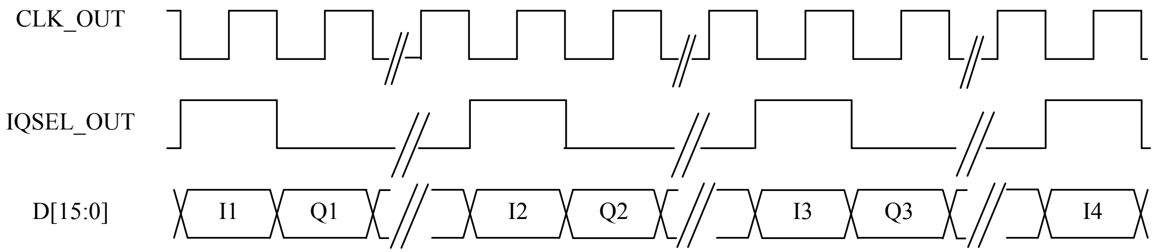


Fig. A-4 DATA timing for UMTS mode and decimate by 2 for 16-bit IQ

Data timing for UMTS modulation mode and decimation ratio of 4

The timing relationships for the DATA interface are as shown in Fig. A-5. The CLK_OUT signal is continuous and remains fixed at 125 MHz, irrespective of the modulation mode and the decimation rate. The ratio of ADC clock rate to IQ sample rate is $\frac{125\,\text{MHz}}{15.36\,\text{MHz}} = 8.14$, a non-integer value that means that data is output sometimes on the 8^{th} clock pulse and sometimes on the 9^{th}. Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

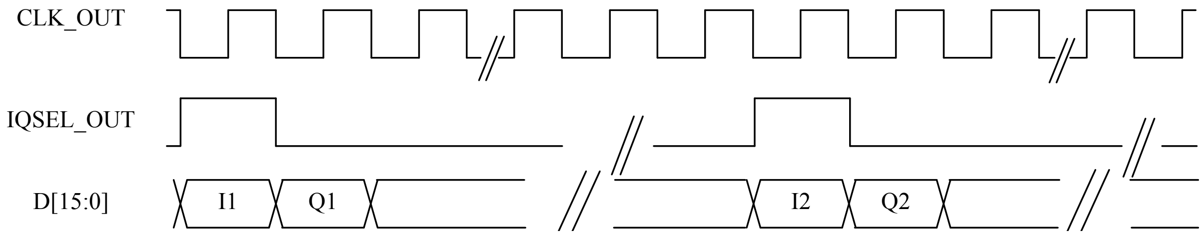


Fig. A-5 DATA timing for UMTS mode and decimate by 4 for 16-bit IQ

Data timing for UMTS modulation mode and decimation ratio of 8

The timing relationships for the DATA interface are as shown in Fig. A-6. The CLK_OUT signal is continuous and remains fixed at 250 MHz, irrespective of the modulation mode and the decimation rate. The ratio of ADC clock rate to IQ sample rate is $\frac{125\text{ MHz}}{7.68\text{ MHz}} = 16.28.$ Therefore the number of clock cycles between IQSELECT_OUT being asserted varies. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

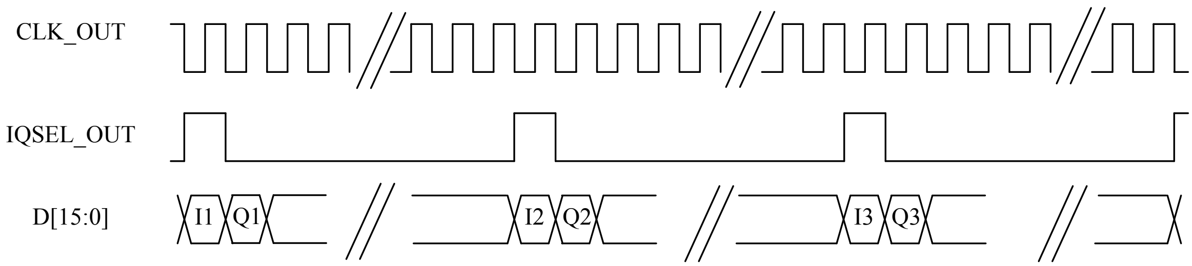


Fig. A-6 DATA timing for 16-bit IQ UMTS mode and decimate by 8

In 32-bit mode, data is transmitted as two 16-bit words, MSW then LSW for I then Q, as shown in Fig. A-7.

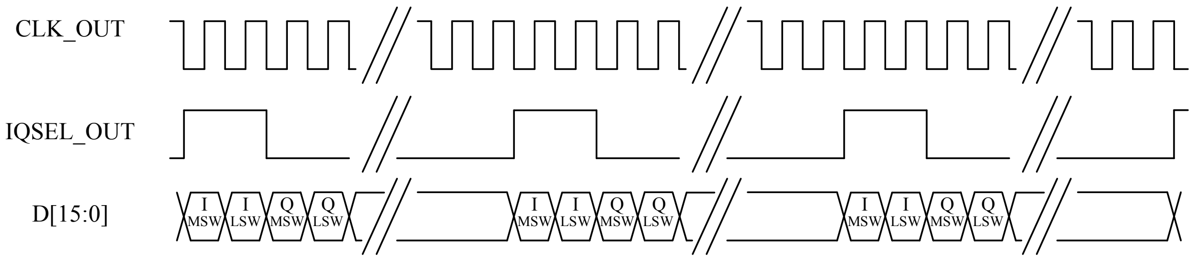


Fig. A-7 DATA timing for 32 bit IQ, UMTS mode and decimate by 8

Data timing for CDMA2000 1X modulation mode

If a modulation mode of CDMA2000 1X and a decimation value of 1 are both selected, IQ data is generated at eight times the CDMA2000 1X chip rate. As the chip rate is 1.2288 MHz, this gives an IQ sample rate of 9.8304 Ms/s. There is no longer an integer relationship between the clock rate of 125 MHz and the 9.8304 Ms/s data rate.

The number of clock cycles between IQSELECT_OUT being asserted is not fixed but varies. This is true for all CDMA mode decimation ratios.

The timing relationship for the DATA interface is shown in Fig. A-8. Note that the CLK_OUT signal is continuous and remains fixed at 125 MHz, irrespective of the modulation mode and the decimation rate. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

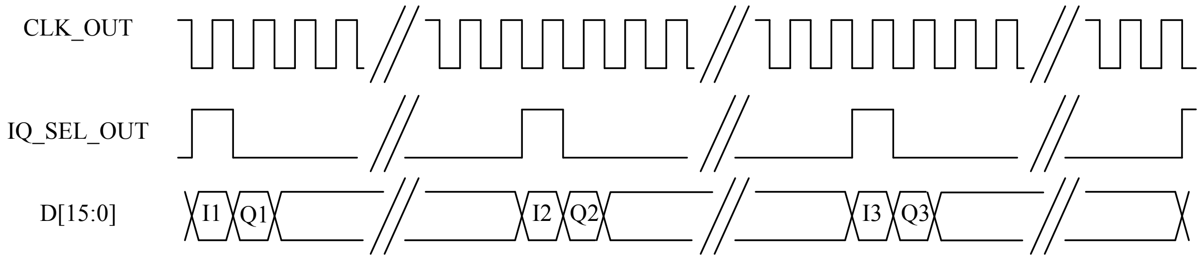


Fig. A-8 DATA timing for CDMA2000 1X

Data transmission for GSM modulation mode and a decimation ratio of 1

In this mode the IQ data is resampled to produce IQ data at 16 times the GSM symbol rate of 270.83 kHz, that is, 4.333 Ms/s. The timing relationships for the DATA interface is as shown in Fig. A-9. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at 125 MHz. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

There is no integer relationship between the data rate of 4.33 MHz and the clock frequency of 125 MHz. Therefore the number of clock cycles between IQSELECT_OUT being asserted is no longer fixed but varies. This is true for all GSM mode decimation ratios.

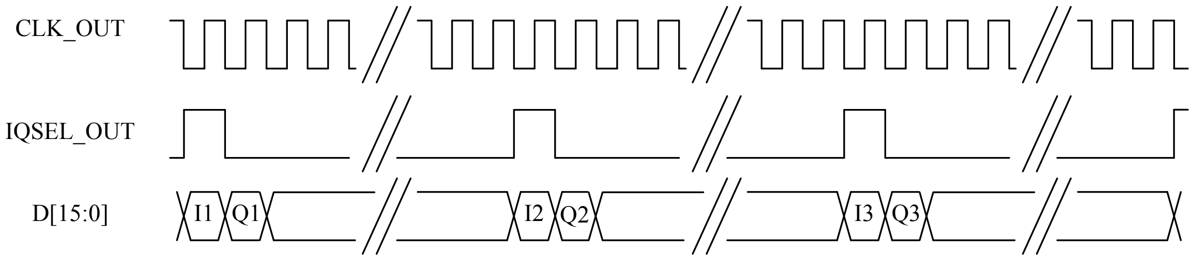


Fig. A-9 DATA timing for GSM for 16-bit IQ

Data transmission for 2319E emulation mode

In this mode, the IQ data is resampled to produce IQ data at 4.08 MHz with a decimation ratio of 16. The timing relationships for the DATA interface are as shown in Fig. A-10. Note that the CLK_OUT signal is continuous and that the frequency of the clock remains fixed at 125 MHz. IQSELECT_OUT is toggled only when an IQ data pair is being transmitted.

There is no integer relationship between the data rate of 4.08 MHz and the clock frequency of 125 MHz. Therefore the number of clock cycles between IQSELECT_OUT being asserted is no longer fixed but varies. This is true for all 2319E modulation mode decimation ratios.

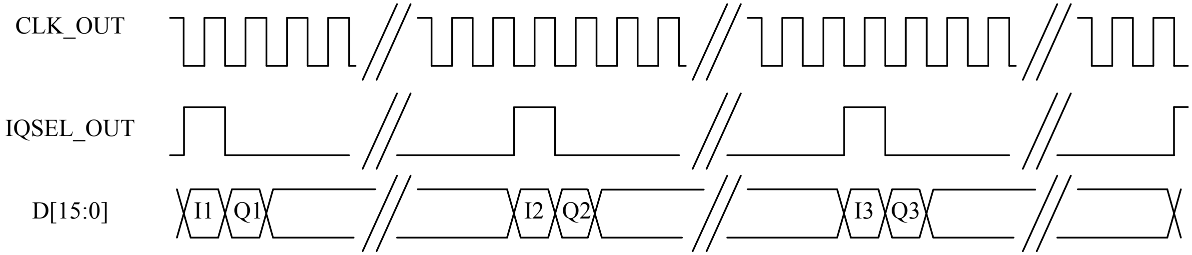


Fig. A-10 DATA timing for 2319 emulation for 16-bit IQ

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